REMARKS

This is in response to the Office Action dated October 6, 2003. Claims 22 and 63 have been canceled. New claims 65-68 have been added. Thus, claims 1-21, 23-62 and 64-68 are now pending.

For purposes of example, and without limitation, certain example embodiments of this invention relate to an imager including an active substrate and an opposing substrate. The active substrate, as shown in Figs. 1-4 for example, includes pixel electrodes 14, storage capacitor electrodes 10 and switching TFTs 5. The opposing substrate includes a photoconductive layer 32 (e.g., comprising CdTe or CdZnTe), carrier blocking layer 18 and charge collecting electrode 6. Each electrically conductive connecting member 3 is located between the substrates and electrically connects the photoconductive layer 32 to a corresponding pixel electrode 14 of the active substrate, via at least charge collecting layer 6. Moreover, space keeping members (i.e., spacers) 45 are laterally separated from the pixel electrodes and are provided for spacing the substrates from one another (e.g., see Figs. 1 and 4). The spacers 45 may be arranged in lattice form in certain example embodiments so as to surround the conductive connecting members 3 (e.g., see Fig. 4).

Double Patenting Rejection

Independent claims 1, 18, 24, 59, and 62 stand rejected under the doctrine of obviousness type double patenting over claim 1 of Izumi '700 in view of Williams. This double patenting rejection is respectfully traversed for at least the following reasons.

Claims 1 and 59 require that the at least one space keeping member is arranged in lattice form. For example, see Fig. 4 of the instant application which illustrates that the at least one space keeping member 45 is in lattice form so as to surround the conductive connecting members 3. The cited art fails to disclose or suggest this "lattice" aspect of claims 1 and 59. Nothing in claim 1 of Izumi '700 or in Williams discloses or suggests the claimed lattice form required by these claims. Thus, it is respectfully submitted that the obviousness-type double patenting rejection of these claims should be withdrawn. See also the *Reasons for Allowance* associated with original claim 2 provided by the Examiner, which indicate that the art fails to disclose or suggest the "lattice" aspect of these claims.

Independent claims 18, 62 and 65 require insulating photosensitive space keeping member(s). Again, nothing in claim 1 of Izumi '700 or in Williams discloses or suggests this aspect of these claims. *See also the Reasons for Allowance provided by the Examiner for claim 5.* Thus, it is respectfully submitted that the obviousness-type double patenting rejection of these claims should be withdrawn.

Moreover, the alleged combination of Izumi '700 and Williams is improper. In particular, Izumi '700 claims a conductive connecting layer for connecting the substrates to one another. The conductive connecting layer of Izumi '700 also spaces the substrates from one another. Thus, one of ordinary skill in the art would never have provided additional space keeping members, separate from the conductive members, in Izumi '700.

The alleged combination is based on impermissible hindsight – since there is clearly no teaching in the art for providing Izumi '700 with additional space keeping members.

Furthermore, Williams relates to IC chip products which use bump electrodes – this is entirely non-analogous to the imagers of Izumi. In other words, the two references relate to entirely diverse subject matters and are not properly combinable. One of ordinary skill in the art would never have used spacers from an IC chip with bumped chips in the imager of Izumi '700. For example, Izumi '700 clearly does not suffer from the problem discussed in Williams relating to the fragility of indium bumped chips. Since Izumi is entirely unrelated to, and does not suffer from, this problem, one of ordinary skill in the art would never have provided Izumi '700 with the stops of Williams which are only designed to facilitate automated processing of indium bumped chips.

For at least these reasons, the obviousness-type double patenting rejection should be withdrawn.

<u>Art Rejections</u>

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Tran in view of Williams. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "at least one space keeping member for keeping a space between the substrates, wherein said at least one space keeping member is arranged in <u>lattice</u> form." For example, see Fig. 4 of the instant application which illustrates that the at least

one space keeping member 45 is in lattice form so as to surround the conductive connecting members 3.

The cited art fails to disclose or suggest this "lattice" aspect of claim 1, either alone or in the alleged combination. Thus, even if the references were combined (which applicant believes would be incorrect in any event), the invention of claim 1 still would not be met. See also the *Reasons for Allowance* associated with original claim 2 provided by the Examiner, which indicate that the art fails to disclose or suggest the "lattice" aspect of this claim. Accordingly, it is clear that claim 1 is now in condition for allowance.

Claim 59 as filed also requires "lattice form." The cited art fails to disclose or suggest this aspect of claim 59, either alone or in the alleged combination. Thus, claim 59 is also in condition for allowance.

Claims 18, 62 and 65 require insulating <u>photosensitive</u> space keeping member(s). Both Tran and Williams fail to disclose or suggest this "photosensitive" aspect of these claims. *See also the Reasons for Allowance provided by the Examiner for claim 5.* Thus, claims 18, 62 and 65 are now in condition for allowance.

Claims 24 and 67 require that the conductive connecting member(s) does not contact any TFT gate. This clearly excludes the unrelated structure of Tran. Tran teaches directly away from the invention of claims 24 and 67, since Tran's alleged conductive member 66 is provided only to connect the TFT gate to the diode. Thus, even

the alleged combination of Tran and Williams fails to meet the inventions of these claims.

Further with respect to claims 24 and 67, the combination of Tran and Williams is incorrect as a matter of law. In particular, Tran relates to a radiation detector including a TFT connected to a diode. On the other hand, Williams relates to IC chip products which use indium bumped chips and suffer from certain problems related thereto. In other words, the two references relate to entirely diverse subject matters and are not properly combinable. One of ordinary skill in the art would never have used spacers from an IC chip with bumped chips in the detector of Tran. For example, Tran clearly does not suffer from the problem discussed in Williams relating to the fragility of indium bumped chips. Since Tran is entirely unrelated to, and does not suffer from, this problem of Williams, one of ordinary skill in the art would never have provided Tran with the stops of Williams which are only designed to facilitate automated processing of indium bumped chips. Thus, the Section 103(a) combination of Tran and Williams appears to be incorrect, and the rejection should be withdrawn for this additional reason.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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